

CLAIMS:

- 1 1. A method for fabricating a semiconducting layer with reduced soft error rates
2 comprising:
3 providing a semiconductor substrate;
4 forming a first semiconductor layer over the substrate, said first semiconductor
5 layer being comprised of a first semiconductor material and having a vertical extent
6 defined by an upper extent of the first semiconductor material and a lower extent of the
7 first semiconductor material;
8 forming a generally constant electric field across the vertical extent of the first
9 semiconductor material, wherein a charge which occurs within the first semiconductor
10 layer is influenced toward the semiconductor substrate; and
11 forming a device layer in which a semiconductor device may be fabricated.
- 1 2. The method for fabricating recited in claim 1 above, wherein forming a first
2 semiconductor layer over the substrate further comprises:
3 establishing a first dopant concentration;
4 establishing a second dopant concentration; and
5 depositing the first semiconductor material in a graded dopant concentration
6 profile, said graded dopant concentration having said first dopant concentration at the
7 lower extent of the semiconductor material, said second dopant concentration at the upper
8 extent of the semiconductor material, and dopant concentrations between said first dopant
9 concentration and said second dopant concentration between the upper extent and lower
10 extent of the first semiconductor material.

1 3. The method for fabricating recited in claim 2 above, wherein establishing said
2 second dopant concentration is based on said semiconductor device to be fabricated in the
3 device layer.

1 4. The method for fabricating recited in claim 2 above, wherein said device layer is
2 formed within the vertical extent of first semiconductor material.

1 5. The method for fabricating recited in claim 3 above further comprises:
2 forming a second electric field at the lower extent of the first semiconductor
3 material.

1 6. The method for fabricating recited in claim 5 above, wherein forming said second
2 electric field further comprises:
3 determining a dopant concentration of said semiconductor substrate;
4 selecting the second dopant concentration based on said dopant concentration of
5 said semiconductor substrate, wherein said second dopant concentration is different from
6 said dopant concentration of said semiconductor substrate.

1 7. The method for fabricating recited in claim 3 above further comprises:
2 forming a second electric field below the first semiconductor material.

1 8. The method for fabricating recited in claim 7 above, wherein said semiconductor
2 substrate is a P+ semiconductor substrate, and forming said second electric field further
3 comprises:
4 forming an undoped intrinsic layer over said P+ semiconductor substrate; and
5 forming said first semiconductor layer over the undoped intrinsic layer.

1 9. The method for fabricating recited in claim 7 above, wherein said semiconductor
2 substrate is a P- semiconductor substrate, and forming said second electric field further
3 comprises:

4 forming a buried n-layer over said P- semiconductor substrate;

5 forming an undoped intrinsic layer over said buried n-layer; and

6 forming said first semiconductor layer over the undoped intrinsic layer.

1 10. The method for fabricating recited in claim 1 above, wherein forming the first
2 semiconductor layer further comprises epitaxially forming the first semiconductor layer.

1 11. A semiconducting structure having reduced with soft error rates comprising:

2 a semiconductor substrate;

3 a first semiconductor layer over the substrate, said first semiconductor layer being
4 comprised of a first semiconductor material and having a vertical extent defined by an
5 upper extent of the first semiconductor material and a lower extent of the first
6 semiconductor material;

7 a generally constant electric field across the vertical extent of the first
8 semiconductor material, wherein a charge which occurs within the first semiconductor
9 layer is influenced toward the semiconductor substrate; and

10 a device layer in which a semiconductor device may be fabricated.

1 12. The semiconducting structure recited in claim 11 above, wherein the first
2 semiconductor layer over the substrate further comprises a graded dopant concentration,
3 said graded dopant concentration having a first dopant concentration established at the
4 lower extent of the semiconductor material, a second dopant concentration established at
5 the upper extent of the semiconductor material and a plurality of dopant concentrations

6 between said first dopant concentration and said second dopant concentration between
7 the upper extent and lower extent of the first semiconductor material.

1 13. The semiconducting structure recited in claim 12 above, wherein said second
2 dopant concentration is based on said semiconductor device to be fabricated in the device
3 layer.

1 14. The semiconducting structure recited in claim 12 above, wherein said device layer
2 is formed within the vertical extent of first semiconductor material.

1 15. The semiconducting structure recited in claim 13 above further comprises:
2 a second electric field formed at the lower extent of the first semiconductor
3 material.

1 16. The semiconducting structure recited in claim 15 above, wherein the second
2 dopant concentration is based on a dopant concentration of said semiconductor substrate,
3 wherein said second dopant concentration is different from said dopant concentration of
4 said semiconductor.

1 17. The semiconducting structure recited in claim 13 above further comprises:
2 a second electric field below the first semiconductor material.

1 18. The semiconducting structure recited in claim 17 above, wherein said
2 semiconductor substrate is a P+ semiconductor substrate, and said semiconducting
3 structure further comprises:

4 an undoped intrinsic layer formed over said P+ semiconductor substrate and under
5 said first semiconductor layer.

- 1 19. The semiconducting structure recited in claim 17 above, wherein said
2 semiconductor substrate is a P- semiconductor substrate, and semiconducting further
3 comprises:
4 a buried n-layer formed over said P- semiconductor substrate; and
5 an undoped intrinsic layer formed over said buried n-layer and formed under said
6 first semiconductor layer.
- 1 20. A method for fabricating recited in claim 11 above, wherein the first
2 semiconductor layer is an epitaxial first semiconductor layer.